AN4612
Application note

Migrating from STM32L1 series to STM32L4 series microcontrollers

Introduction

For designers of STM32 microcontroller applications, it is important to be able to easily replace one microcontroller type by another one in the same product family. Migrating an application to a different microcontroller is often needed, when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. On the other hand, cost reduction objectives may also be an argument to switch to smaller components and shrink the PCB area.

This application note is written to help analyzing the steps required to migrate an existing design from STM32L1 series to STM32L4 series. It groups together the most important information and lists the vital aspects that need to be addressed.

This document lists the “full set” of features available for the STM32L1 and STM32L4 series (some products may have less features depending on their part number).

In order to migrate an application from STM32L1 series to STM32L4 series, these three aspects need to be considered: the hardware migration, the peripheral migration and the firmware migration.

To fully benefit from the information in this application note, the user should be familiar with the STM32 microcontrollers documentation available on *www.st.com*, with a particular focus on:

STM32L1 series:

- STM32L1xx reference manual (RM0038)
- STM32L1xx datasheets
- STM32L1 Flash and EEPROM programming manual (PM0062).

STM32L4 series:

- STM32L4x6 reference manual (RM0351)
- STM32L4xx datasheets.

Table 1. Applicable products

Type	Applicable products
Microcontrollers	STM32L1 series, STM32L4 series.

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1 STM32L4 series overview

The STM32L4 series forms a perfect fit in terms of ultra-low-power, performances, memory size, and peripherals at a cost effective price.

In particular, the STM32L4 series allows higher frequency/performance operation than STM32L1 series, including a Cortex®-M4 @80 MHz versus Cortex®-M3 @32 MHz and optimized Flash memory access through the adaptive real-time memory accelerator (ART Accelerator™).

The STM32L4 series includes a larger set of peripherals with advanced features and optimized power consumption compared to the STM32L1.

STM32L4 increases low-power efficiency in dynamic mode (µA/MHz) still reaching very low level of static power consumption on various available low-power modes.

The detailed list of available features and packages for each product can be found in the respective datasheet.

2 Hardware migration

The ultra-low-power STM32L4 and STM32L1 series present a high level of pin compatibility. Most peripherals share the same pins in the two series.

The transition from the STM32L1 series to the STM32L4 series for QFP and BGA packages is easy since only a few pins are different (refer to *Table 2* and *Table 3*).

For the WLCSP packages the transition is less easy because the pinout is different. This is due to the fact that devices of STM32L1 series and STM32L4 series have different die sizes.

Table 2. STM32L1 series and STM32L4 series pinout differences (QFP)

STM32L1 series				STM32L4 series			
QFP64	**QFP100**	**QFP144**	**Pinout**	**QFP64**	**QFP100**	**QFP144**	**Pinout**
1	6	6	VLCD	1	6	6	VBAT
-	-	95	VDD	-	-	95	VDDIO2(1)
-	-	131	VDD	-	-	131	VDDIO2(1)
-	73	106	PH2	-	73	106	VDDUSB
48	-	-	VDD	48	-	-	VDDUSB

1. VDDIO2 pin can be connected externally to V_{DD}.

Table 3. STM32L1 series and STM32L4 series pinout differences (BGA)

STM32L1 series		STM32L4 series	
BGA132	**Pinout**	**BGA132**	**Pinout**
E2	VLCD	E2	VBAT
G7	VDD	G7	VDDIO2(1)
C11	PH2	C11	VDDUSB
G3	PF6	G3	PG11
G4	PF7	G4	PG6
H4	PF8	H4	PG7
J6	PF9	J6	PG8
K1	NC	K1	PG15

1. VDDIO2 pin can be connected externally to V_{DD}.

Recommendations to migrate from STM32L1 series board to a STM32L4 series board

VLCD pin in STM32L4 series is now multiplexed on PC3 GPIO (pin 29 on QFP144, pin 18 on QFP100, pin 11 on QFP64, pin K2 on BGA132) through alternate function programming in STM32L4 series.

This implies that other functions in STM32L4 series PC3 pins cannot be used on PC3 when LCD is used by the application.

This also implies that the STM32L1 series PC3 related alternate functions, if used by the application, should be mapped onto other STM32L4 series pins.

V_{BAT} or V_{DD} supply (if no specific V_{BAT} power is used), should now be connected to:

- pin 6 (QFP144 and QFP100)
- pin 1 (QFP64)
- pin E2 (BGA132).

V_{DDUSB} supply should now be connected to GPIO PH2:

- pin 106 (QFP144)
- pin 73 (QFP100)
- pin C11 (BGA132)

GPIO PH2 cannot be used as regular GPIO anymore (no PH2 GPIO in STM32L4 series).

On BGA132, several GPIOs from STM32L1 series are mapped on different GPIOs in STM32L4 series:

- PF6 (pin G3) mapped to PG11 on same pin
- PF7 (pin G4) mapped to PG6 on same pin
- PF8 (pin H4) mapped to PG7 on same pin
- PF9 (pin J6) mapped to PG8 on same pin

Also not connected (NC) pin K1 in STM32L1 series can now be used as GPIO PG15 in STM32L4 series.

The figures below show examples of board designs migrating from STM32L1 series to STM32L4 series.

Figure 1. LQFP144 compatible board design

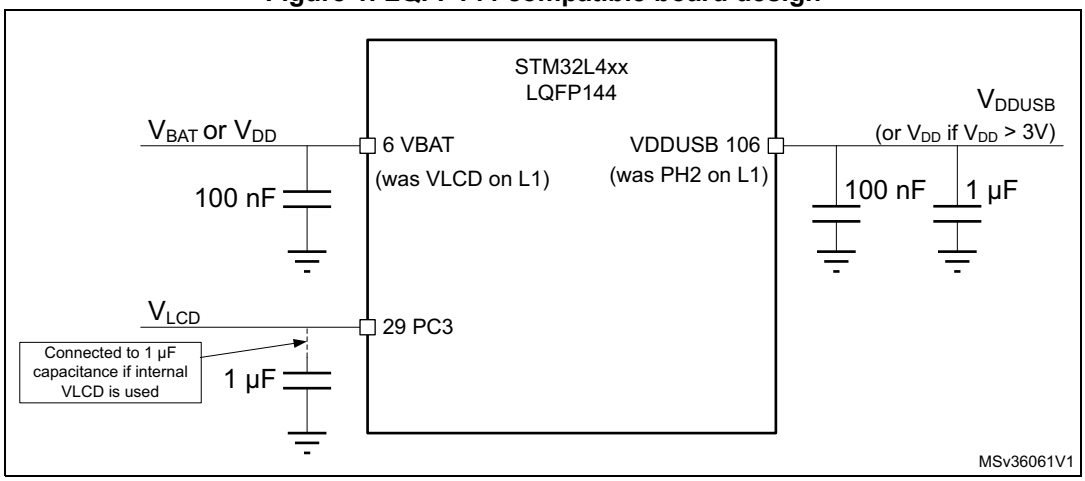


Figure 2. LQFP100 compatible board design

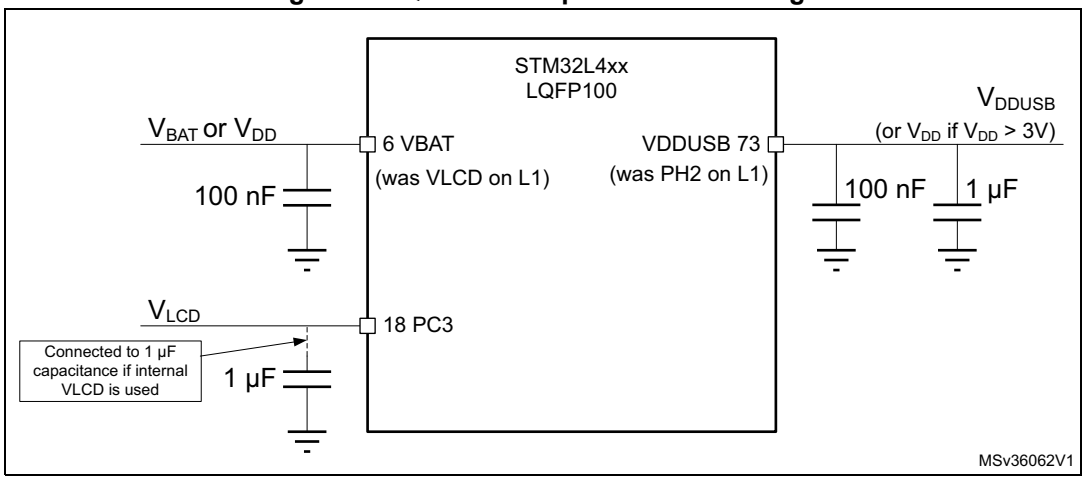


Figure 3. LQFP64 compatible board design

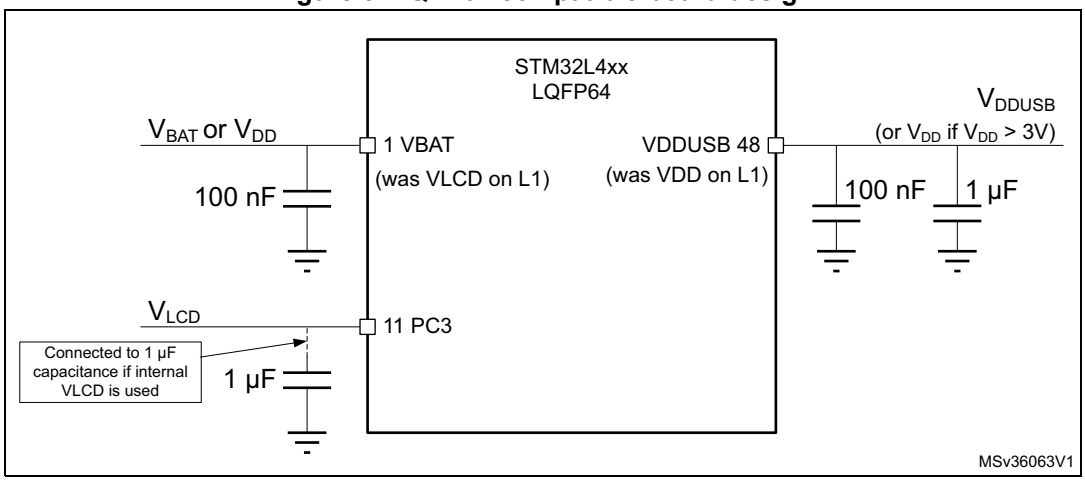
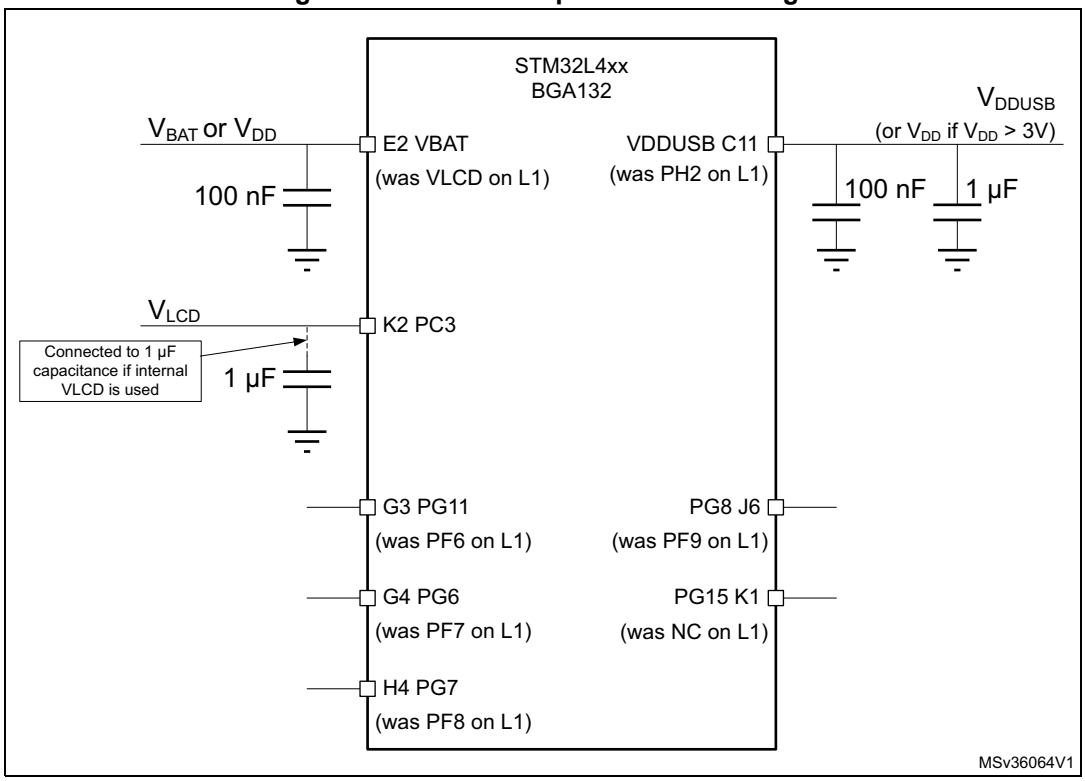


Figure 4. BGA132 compatible board design



3 Boot mode selection

The way to select the boot mode differs between the STM32L1 and the STM32L4 series. On the STM32L1 series the boot mode is selected with two pins. In STM32L4 series the boot mode is selected with one pin and the nBOOT1 option bit located in the user option bytes at memory address 0x1FFF7800. For both STM32L1 and STM32L4 series, the boot mode can be selected among these three options: boot from main Flash memory, boot from SRAM or boot from system memory.

Table 4 summarizes the different configurations available for selecting the boot mode.

Table 4. Boot modes

L4/L1 boot mode selection		Boot mode	Aliasing
BOOT1(1)	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

1. The BOOT1 value is the opposite of the nBOOT1 option bit.

Embedded bootloader

The embedded bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces:

Table 5. Bootloader interfaces

Peripheral	Pin	STM32L1	STM32L4
DFU	USB_DM (PA11) USB_DP (PA12)	X	X
USART1	USART1_TX (PA9) USART1_RX (PA10)	X	X
USART2	USART2_TX (PD5) USART2_RX (PD6)	X	-
USART2	USART2_TX (PA2) USART2_RX (PA3)	-	X
USART3	USART3_TX (PC10) USART3_RX (PC11)	-	X
I2C1	I2C1_SCL (PB6) I2C1_SDA (PB7)	-	X
I2C2	I2C2_SCL (PB10) I2C2_SDA (PB11)	-	X

Table 5. Bootloader interfaces (continued)

Peripheral	Pin	STM32L1	STM32L4
I2C3	I2C3_SCL (PC0) I2C3_SDA (PC1)	-	X
SPI1	SPI1_NSS (PA4) SPI1_SCK (PA5) SPI1_MISO (PA6) SPI1_MOSI (PA7)	-	X
SPI2	SPI2_NSS (PB12) SPI2_SCK (PB13) SPI2_MISO (PB14) SPI2_MOSI (PB15)	-	X
SPI3	SPI3_NSS (PA15) SPI3_SCK (PC10) SPI3_MISO (PC11) SPI3_MOSI (PC12)	-	X

Please refer to AN2606 for more details on the bootloader.

4 Peripheral migration

4.1 STM32 product cross-compatibility

The STM32 series embeds a set of peripherals which can be classified in three categories:

- The first category is for the peripherals that are common to all products. Those peripherals are identical on all products, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second category is for the peripherals that present minor differences from one product to another (usually differences due to the support of new features). Migrating from one product to another is very easy and does not require any significant new development effort.
- The third category is for peripherals which have been considerably modified from one product to another (new architecture, new features...). For this category of peripherals, migration will require new development at application level.

Table 6 gives a general overview of this classification.

The “software compatibility” mentioned in the table below only refers to the register description for “low level” drivers.

The STMCube™ hardware abstraction layer (HAL) between STM32L1 and STM32L4 series is compatible.

Table 6. Peripheral compatibility analysis STM32L1 series versus STM32L4 series

Peripheral	Nb inst. in L1	Nb inst. in L4	Compatibility (migrating from STM32L1 series to STM32L4 series)		
			Software	Pinout	Comments
SPI **I2S**	3 0	3 2	Partial compatibility	Partial compatibility	I2S is no more supported by SPI but replaced by dedicated Serial Audio Interface (SAI) in STM32L4 series. Some alternate function not mapped on same GPIO for SPI1.
WWDG	1	1	Full Compatibility	NA	-
IWDG	1	1	Full Compatibility	NA	-
DBGMCU	1	1	Full Compatibility	NA	-
CRC	1	1	Partial compatibility	NA	Additional features in STM32L4 series.
EXTI	1	1	Partial compatibility	Full compatibility	Only PH2 GPIO not available as EXTI input in STM32L4 series.
USB	1	1	No compatibility	Full compatibility	New peripheral (USB FS in STM32L1 series, USB OTG FS in STM32L4 series).
DMA	1	2	Full Compatibility	NA	Same features. DMA mapping request may differ (see *Section 4.3: DMA*).

Table 6. Peripheral compatibility analysis STM32L1 series versus STM32L4 series (continued)

Peripheral	Nb inst. in L1	Nb inst. in L4	Compatibility (migrating from STM32L1 series to STM32L4 series)		
			Software	Pinout	Comments
TIM Basic General P. Advanced Low-power	9 2 7 - -	13 2 7 2 2	Full Compatibility	Partial compatibility	Some pins not mapped on same GPIO. Timer instance name may differ. Internal connections may differ.
SDIO	1	1	Full Compatibility	Partial compatibility	Some pins not mapped on same GPIO.
FSMC/ FMC	1	1	Full Compatibility	Full Compatibility	Only SRAM/NOR supported in STM32L1 series. NAND supported in STM32L4 series.
PWR	1	1	Partial compatibility	NA	-
RCC	1	1	Partial compatibility	NA	-
USART	3	3	Partial compatibility	Full Compatibility	Additional features in STM32L4 series.
UART	2	2 1 (LP)	Partial compatibility	Full Compatibility	Additional features in STM32L4 series. Additional LPUART in STM32L4 series.
I2C	2	3	No compatibility	Full Compatibility	Additional features in STM32L4 series.
DAC	2	2	Partial compatibility	Full Compatibility	Additional features in STM32L4 series. SW compatible except for output buffer management.
ADC	1	3	No compatibility	Partial compatibility	Additional features in STM32L4 series. Some pins mapped on different GPIOs.
RTC	1	1	Partial compatibility	Full Compatibility	Additional features in STM32L4 series. Can be powered by VBAT in STM32L4 series.
FLASH	1	1	No compatibility	NA	New peripheral.
GPIO	Up to 115 IOs	Up to 114 IOs	Full compatibility	Partial compatibility	at Reset, STM32L1 series configured in input floating mode, STM32L4 series in analog mode. A few changes mentioned in *Section 2: Hardware migration*. No PH2 GPIO in STM32L4 series.
LCD glass	1	1	Full compatibility	Partial compatibility	VLCD muxed on PC3 GPIO. SEG21 not mapped on same GPIO. Additional features in STM32L4 series.
COMP	2	2	No compatibility	Partial compatibility	Some pins mapped on different GPIOs.
SYSCFG	1	1	Partial compatibility	NA	-
AES	1	1	Full compatibility	NA	Additional features in STM32L4 series.

Table 6. Peripheral compatibility analysis STM32L1 series versus STM32L4 series (continued)

Peripheral	Nb inst. in L1	Nb inst. in L4	Compatibility (migrating from STM32L1 series to STM32L4 series)		
			Software	Pinout	Comments
OPAMP	3	2	No compatibility	Partial compatibility	Some pins not mapped on same GPIO. One less OPAMP in STM32L4 series.

Color key:

= No compatibility (new feature or new architecture)

= Partial compatibility (minor changes)

= Full Compatibility (from STM32L1 series to STM32L4 series)

= not applicable

4.2 Memory mapping

The peripheral address mapping has been changed in the STM32L4 series versus the STM32L1 series.

The table below provides the peripheral address mapping correspondence between STM32L1 and STM32L4 series.

Table 7. Peripheral address mapping differences between STM32L1 series and STM32L4 series

Peripheral	STM32L1 series		STM32L4 series	
	Bus	Base address	Bus	Base address
FSMC (FMC in STM32L4 series)	AHB	0xA0000000	AHB3	0xA0000000
AES		0x50060000	AHB2	0x50060000
DMA2		0x40026400	AHB1	0x40020400
DMA1		0x40026000		0x40020000
Flash memory Interface		0x40023C00		0x40022000
RCC		0x40023800		0x40021000
CRC		0x40023000		0x40023000
GPIOG		0x40021C00	AHB2	0x48001800
GPIOF		0x40021800		0x48001400
GPIOH		0x40021400		0x48001C00
GPIOE		0x40021000		0x48001000
GPIOD		0x40020C00		0x48000C00
GPIOC		0x40020800		0x48000800
GPIOB		0x40020400		0x48000400
GPIOA		0x40020000		0x48000000
USART1	APB2	0x40013800	APB2	0x40013800
SP1		0x40013000		0x40013000
SDIO (SDMMC in STM32L4 series)		0x40012C00		0x40012800
ADC1 (ADC123 in STM32L4 series)		0x40012400	AHB2	0x50040000
TIM11		0x40011000	NA	
TIM10		0x40010C00		
TIM9		0x40010800		
EXTI		0x40010400	APB2	0x40010400
SYSCFG		0x40010000		0x40010000

Table 7. Peripheral address mapping differences between STM32L1 series and STM32L4 series (continued)

Peripheral	STM32L1 series		STM32L4 series	
	Bus	Base address	Bus	Base address
COMP	APB1	0x40007C00	APB2	0x40010200
RI		0x40007C04	NA	
OPAMP		0x40007C5C	APB1	0x40007800
DAC		0x40007400	APB1	0x40007400
PWR		0x40007000		0x40007000
USB device FS SRAM		0x40006000	NA	
USB device FS		0x40005C00		
I2C2		0x40005800	APB1	0x40005800
I2C1		0x40005400		0x40005400
USART5 (UART5 in STM32L4 series)		0x40005000		0x40005000
USART4 (UART4 in STM32L4 series)		0x40004C00		0x40004C00
USART3		0x40004800		0x40004800
USART2		0x40004400		0x40004400
SPI3		0x40003C00		0x40003C00
SPI2		0x40003800		0x40003800
IWDG		0x40003000		0x40003000
WWDG		0x40002C00		0x40002C00
RTC (inc. BKP registers)		0x40002800		0x40002800
LCD		0x40002400		0x40002400
TIM7		0x40001400		0x40001400
TIM6		0x40001000		0x40001000
TIM5		0x40000C00		0x40000C00
TIM4		0x40000800		0x40000800
TIM3		0x40000400		0x40000400
TIM2		0x40000000		0x40000000

Table 7. Peripheral address mapping differences between STM32L1 series and STM32L4 series (continued)

Peripheral	STM32L1 series		STM32L4 series	
	Bus	Base address	Bus	Base address
Peripherals available in STM32L4 series and not available in STM32L1 series				
RNG	NA		AHB2	0x50060800
USB OTG FS				0x50000000
TSC			AHB1	0x40024000
DFSDM			APB2	0x40016000
SAI2				0x40015800
SAI1				0x40015400
TIM17				0x40014800
TIM16				0x40014400
TIM15				0x40014000
TIM8				0x40013400
TIM1				0x40012C00
FIREWALL				0x40011C00
VREF				0x40010030
LPTIM2			APB1	0x40009400
SWPMI1				0x40008800
LPUART1				0x40008000
LPTIM1				0x40007C00
CAN1				0x40006400
I2C3				0x40005C00
QUADSPI			AHB3	0xA0001000
Color key: = base address or bus change = not applicable				

The system memory mapping has been updated between STM32L1 and STM32L4 series, please refer to reference manual or datasheet for more details.

The STM32L4 series features an additional SRAM (SRAM2) of 32 Kbyte. The SRAM2 includes additional features listed below:

- Maximum performance through ICode bus access without physical remap
- Parity check option (32-bit + 4-bit parity check)
- Write protection with 1 Kbyte granularity
- Read Protection (RDP)
- Erase by system reset (option byte) or by software
- Content is preserved in Low-power run, Low-power sleep, Stop 0, Stop 1, Stop 2 mode
- **Content can be preserved (RRS bit set in PWR_CR3 register) in Standby mode (not the case for SRAM1).**

4.3 DMA

STM32L1 and STM32L4 series use the same DMA controller fully compatible.

STM32L1 and STM32L4 series embed two DMA controllers, up to 7+5 channels for STM32L1 series and 7+7 channels for STM32L4 series. Each channel is dedicated to managing memory access requests from one or more peripherals. It has an arbiter for handling the priority between DMA requests.

The table below presents the correspondence between the DMA requests of the peripherals in STM32L1 series and STM32L4 series.

Table 8. DMA request differences migrating STM32L1 series to STM32L4 series

Peripheral	DMA request	STM32L1 series	STM32L4 series
ADC1	**ADC1**	DMA1_Channel1	DMA1_Channel1 DMA2_Channel3
DAC	**DAC_Channel1** **DAC_Channel2** **DAC1** **DAC2**	DMA1_Channel2 (1) DMA1_Channel3 (1) NA NA	NA NA DMA1_Channel3 DMA2_Channel4 DMA1_Channel4 DMA2_Channel5
SPI1	**SPI1_Rx** **SPI1_Tx**	DMA1_Channel2 DMA1_Channel3	DMA1_Channel2 DMA2_Channel3 DMA1_Channel3 DMA2_Channel4
SPI2	**SPI2_Rx** **SPI2_Tx**	DMA1_Channel4 DMA1_Channel5	DMA1_Channel4 DMA1_Channel5
SPI3	**SPI3_Rx** **SPI3_Tx**	DMA2_Channel1 DMA2_Channel2	DMA2_Channel1 DMA2_Channel2
USART1	**USART1_Rx** **USART1_Tx**	DMA1_Channel5 DMA1_Channel4	DMA1_Channel5 DMA2_Channel7 DMA1_Channel4 DMA2_Channel6
USART2	**USART2_Rx** **USART2_Tx**	DMA1_Channel6 DMA1_Channel7	DMA1_Channel6 DMA1_Channel7
USART3	**USART3_Rx** **USART3_Tx**	DMA1_Channel3 DMA1_Channel2	DMA1_Channel3 DMA1_Channel2
UART4	**UART4_Rx** **UART4_Tx**	DMA2_Channel3 DMA2_Channel5	DMA2_Channel5 DMA2_Channel3
UART5	**UART5_Rx** **UART5_Tx**	DMA2_Channel2 DMA2_Channel1	DMA2_Channel2 DMA2_Channel1
I2C1	**I2C1_Rx** **I2C1_Tx**	DMA1_Channel7 DMA1_Channel6	DMA1_Channel7 DMA2_Channel6 DMA1_Channel6 DMA2_Channel7

Table 8. DMA request differences migrating STM32L1 series to STM32L4 series

Peripheral	DMA request	STM32L1 series	STM32L4 series
I2C2	**I2C2_Rx** **I2C2_Tx**	DMA1_Channel5 DMA1_Channel4	DMA1_Channel5 DMA1_Channel4
SDIO **SDMMC**	**SDIO** **SDMMC**	DMA2_Channel4 NA	NA DMA2_Channel4 DMA2_Channel5
TIM2	**TIM2_UP** **TIM2_CH1** **TIM2_CH2** **TIM2_CH3** **TIM2_CH4**	DMA1_Channel2 DMA1_Channel5 DMA1_Channel7 DMA1_Channel1 DMA1_Channel7	DMA1_Channel2 DMA1_Channel5 DMA1_Channel7 DMA1_Channel1 DMA1_Channel7
TIM3	**TIM3_UP** **TIM3_CH1** **TIM3_TRIG** **TIM3_CH3** **TIM3_CH4**	DMA1_Channel3 DMA1_Channel6 DMA1_Channel6 DMA1_Channel2 DMA1_Channel3	DMA1_Channel3 DMA1_Channel6 DMA1_Channel6 DMA1_Channel2 DMA1_Channel3
TIM4	**TIM4_UP** **TIM4_CH1** **TIM4_CH2** **TIM4_CH3**	DMA1_Channel7 DMA1_Channel1 DMA1_Channel4 DMA1_Channel5	DMA1_Channel7 DMA1_Channel1 DMA1_Channel4 DMA1_Channel5
TIM5	**TIM5_UP** **TIM5_CH1** **TIM5_CH2** **TIM5_CH3** **TIM5_CH4** **TIM5_TRIG** **TIM5_COM**	DMA2_Channel2 DMA2_Channel5 DMA2_Channel4 DMA2_Channel2 DMA2_Channel1 DMA2_Channel1 DMA2_Channel1	DMA2_Channel2 DMA2_Channel5 DMA2_Channel4 DMA2_Channel2 DMA2_Channel1 DMA2_Channel1 DMA2_Channel1
TIM6	**TIM6_UP**	DMA1_Channel2	DMA1_Channel3 DMA2_Channel4
TIM7	**TIM7_UP**	DMA1_Channel3	DMA1_Channel4 DMA2_Channel5
AES	**AES_OUT** **AES_IN**	DMA2_Channel3 DMA2_Channel5	DMA2_Channel3 DMA2_Channel2 DMA2_Channel5 DMA2_Channel1
Color key: = Differences between STM32L1 and STM32L4 series			

1. For High-density value line devices, the DAC DMA requests are mapped respectively on DMA1 Channel 3 and DMA1 Channel 4.

4.4 Interrupts

The table below presents the interrupt vectors in the STM32L4 series versus the STM32L1 series.

Table 9. Interrupt vector differences between STM32L1 series and STM32L4 series

Position	STM32L1			STM32L4 series
	Cat.1 and Cat.2	Cat.3	Cat.4 and Cat.5	
0	WWDG			WWDG
1	PVD			PVD / PVM
2	TAMPER_ STAMP			TAMPER / CSS
3	RTC_WKUP			RTC_WKUP
4	FLASH			FLASH
5	RCC			RCC
6	EXTI0			EXTI0
7	EXTI1			EXTI1
8	EXTI2			EXTI2
9	EXTI3			EXTI3
10	EXTI4			EXTI4
11	DMA1_Channel1			DMA1_Channel1
12	DMA1_Channel2			DMA1_Channel2
13	DMA1_Channel3			DMA1_Channel3
14	DMA1_Channel4			DMA1_Channel4
15	DMA1_Channel5			DMA1_Channel5
16	DMA1_Channel6			DMA1_Channel6
17	DMA1_Channel7			DMA1_Channel7
18	ADC1			ADC1_2
19	USB_HP			CAN1_TX
20	USB_LP			CAN1_RX0
21	DAC			CAN1_RX1
22	COMP, TSC (1)	COMP/CA		CAN1_SCE
23	EXTI9_5			EXTI9_5
24	LCD			TIM1_BRK / TIM15
25	TIM9			TIM1_UP / TIM16
26	TIM10			TIM1_TRG_COM / TIM17
27	TIM11			TIM1_CC

Table 9. Interrupt vector differences between STM32L1 series and STM32L4 series (continued)

Position	STM32L1			STM32L4 series
	Cat.1 and Cat.2	Cat.3	Cat.4 and Cat.5	
28	TIM2			TIM2
29	TIM3			TIM3
30	TIM4			TIM4
31	I2C1_EV			I2C1_EV
32	I2C1_ER			I2C1_ER
33	I2C2_EV			I2C2_EV
34	I2C2_ER			I2C2_ER
35	SPI1			SPI1
36	SPI2			SPI2
37	USART1			USART1
38	USART2			USART2
39	USART3			USART3
40	EXTI15_10			EXTI15_10
41	RTC_Alarm			RTC_Alarm
42	USB_FS_WKUP			DFSDM4
43	TIM6			TIM8_BRK
44	TIM7			TIM8_UP
45	NA	TIM5	SDIO	TIM8_TRG_COM
46	NA	SPI3	TIM5	TIM8_CC
47	NA	DMA2_Channel1	SPI3	ADC3
48	NA	DMA2_Channel2	UART4	FMC
49	NA	DMA2_Channel3	UART5	SDMMC
50	NA	DMA2_Channel4	DMA2_Channel1	TIM5
51	NA	DMA2_Channel5	DMA2_Channel2	SPI3
52	NA	AES	DMA2_Channel3	UART4
53	NA	COMP_ACQ	DMA2_Channel4	UART5
54	NA		DMA2_Channel5	TIM6_DACUNDER
55	NA		AES	TIM7
56	NA		COMP_ACQ	DMA2_Channel1
57	NA			DMA2_Channel2
58	NA			DMA2_Channel3
59	NA			DMA2_Channel4

Table 9. Interrupt vector differences between STM32L1 series and STM32L4 series (continued)

Position	STM32L1			STM32L4 series
	Cat.1 and Cat.2	Cat.3	Cat.4 and Cat.5	
60	NA			DMA2_Channel5
61	NA			DFSDM1
62	NA			DFSDM2
63	NA			DFSDM3
64	NA			COMP
65	NA			LPTIM1
66	NA			LPTIM2
67	NA			OTG_FS
68	NA			DMA2_CH6
69	NA			DMA2_CH7
70	NA			LPUART1
71	NA			QUADSPI
72	NA			I2C3_EV
73	NA			I2C3_ER
74	NA			SAI1
75	NA			SAI2
76	NA			SWPMI1
77	NA			TSC
78	NA			LCD
79	NA			AES
80	NA			RNG
81	NA			FPU

Color key:

= Different interrupt vector

= Interrupt Vector name changed but STM32L4 series peripheral still mapped on the same interrupt Vector position in STM32L1 series

1. Depending on the product line used.

4.5 RCC

The main differences related to the RCC (reset and clock controller), between the STM32L4 series and the STM32L1 series, are presented in the table below.

Table 10. RCC differences between STM32L1 and STM32L4 series

RCC	STM32L1 series	STM32L4 series
MSI	Multi Speed RC factory and user trimmed (64 kHz, 128 kHz, 256 kHz, 512 kHz, 1.02 MHz, 2.05 MHz, 4.1 MHz)	MSI is a low power oscillator with programmable frequency up to 48 MHz. It can replace PPLs as system clock (faster wakeup, lower consumption). It can be used as USB device clock (no need for external high speed crystal oscillator). Multi Speed RC factory and user trimmed (100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz) Auto calibration from LSE
HSI	16 MHz RC factory and user trimmed	
LSI	37 kHz RC	32 kHz RC Lower consumption, higher accuracy (refer to product datasheet)
HSE	1 - 24 MHz	4 - 48 MHz
LSE	32.768 kHz	32.768 kHz Configurable drive/consumption Available in backup domain (VBAT)
PLL	– Main PLL for system PLL clock sources: HSI, HSE.	– Main PLL for system – 2 PLLs for SAI1/2, ADC, RNG, SDMMC and OTG FS clock. Each PLL can provide up to 3 independent outputs. The PLL multiplication/division factors are different from STM32L1 series. PLL clock sources: MSI, HSI16, HSE.
System clock source	MSI, HSI, HSE or PLL	
System clock frequency	Up to 32 MHz 2 MHz after reset using MSI	Up to 80 MHz 4 MHz after reset using MSI
AHB frequency	Up to 32 MHz	Up to 80 MHz
APB1 frequency	Up to 32 MHz	Up to 80 MHz
APB2 frequency	Up to 32 MHz	Up to 80 MHz

Table 10. RCC differences between STM32L1 and STM32L4 series (continued)

RCC	STM32L1 series	STM32L4 series
RTC clock source	LSI, LSE or HSE clock divided by 2, 4, 8 or 16	LSI, LSE or HSE/32
MCO clock source	– MCO pin (PA8): SYSCLK, HSI, HSE, PLLCLK, MSI, LSE or LSI. With configurable prescaler, 1, 2, 4, 8 or 16 for each output.	
CSS	– CSS (Clock Security System) – CSS on LSE	
Internal oscillator measurement / calibration	– LSE connected to TIM9 or TIM10 CH1 IC: can measure HSI or MSI with respect to LSE clock high precision – LSI connected to TIM10 CH1 IC: can measure LSI with respect to HSI or HSE clock precision – HSE connected to TIM11 CH1 IC: can measure HSE with respect to LSE/HSI clock – MSI connected to TIM11 CH1 IC: can measure MSI with respect to HSI/HSE clock	(mainly replacing TIM9/10/11 in STM32L1 series by TIM15/16/17 in STM32L4 series) – LSE connected to TIM15 or TIM16 CH1 IC: can measure HSI16 or MSI with respect to LSE clock high precision – LSI connected to TIM16 CH1 IC: can measure LSI with respect to HSI16 or HSE clock precision – HSE/32 connected to TIM17 CH1 IC: can measure HSE with respect to LSE/HSI16 clock – MSI connected to TIM17 CH1 IC: can measure MSI with respect to HSI16/HSE clock
Interrupt	– CSS (linked to NMI IRQ) – LSECSS – LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY (linked to RCC global IRQ)	– CSS (linked to NMI IRQ) – LSECSS – LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY, *PLLSAI1RDY* and *PLLSAI2RDY* (linked to RCC global IRQ)
Color key: = New feature or new architecture (difference between STM32L1 and STM32L4 series) = Same feature, but specification change or enhancement		

In addition to the differences described in the table above, the following additional adaptation steps may be needed for the migration.

4.5.1 Performance versus V_{CORE} ranges

The maximum system clock frequency and Flash memory wait state depend on the selected voltage range V_{CORE} and also on V_{DD} for STM32L1 series. The following table gives the different clock source frequencies depending on the product voltage range.

Table 11. Performance versus V_{CORE} ranges

CPU performance	Power performance	V_{CORE} range	Typical Value (V)	Max frequency (MHz)					V_{DD} range
				4 WS	3 WS	2 WS	1 WS	0 WS	
STM32L1									
High	Low	1	1.8	-	-	-	32	16	2.0 - 3.6
Medium	Medium	2	1.5	-	-	-	16	8	1.65 - 3.6
Low	High	3	1.2	-	-	-	4	2	
STM32L4									
High	Medium	1	1.2	80	64	48	32	16	NA
Medium	High	2	1.0	26	26	18	12	6	NA

4.5.2 *Peripheral access configuration*

Since the address mapping of some peripherals has been changed in the STM32L4 series versus the STM32L1 series, different registers need to be used to [enable/disable] or [enter/exit] the peripheral [clock] or [from reset mode].

Table 12. RCC registers used for peripheral access configuration

Bus	Register L1 series	Register L4 series	Comments
AHB	RCC_AHBRSTR	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2) RCC_AHB3RSTR (AHB3) (1)	Used to [enter/exit] the AHB peripheral from reset
	RCC_AHBENR	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2) RCC_AHB3ENR (AHB3) (1)	Used to [enable/disable] the AHB peripheral clock
	RCC_AHBLPENR	RCC_AHB1SMENR (AHB1) RCC_AHB2SMENR (AHB2) RCC_AHB3SMENR (AHB3) (1)	Used to [enable/disable] the AHB peripheral clock in sleep mode
APB1	RCC_APB1RSTR	RCC_APB1RSTR1 RCC_APB1RSTR2 (1)	Used to [enter/exit] the APB1 peripheral from reset
	RCC_APB1ENR	RCC_APB1ENR1 RCC_APB1ENR2 (1)	Used to [enable/disable] the APB1 peripheral clock
	RCC_APB1LPENR	RCC_APB1SMENR1 RCC_APB1SMENR2 (1)	Used to [enable/disable] the APB1 peripheral clock in sleep mode
APB2	RCC_APB2RSTR	RCC_APB2RSTR	Used to [enter/exit] the APB2 peripheral from reset
	RCC_APB2ENR	RCC_APB2ENR	Used to [enable/disable] the APB2 peripheral clock
	RCC_APB2LPENR	RCC_APB2SMENR	Used to [enable/disable] the APB2 peripheral clock in sleep mode

1. The register configuring the peripherals is not present in STM32L1 series, so it should not be needed from a migration-only stand point

The configuration to access a given peripheral involves:

- identifying the bus to which the peripheral is connected, refer to *Table 7 on page 16*
- selecting the right register according the needed action, refer to *Table 12* above.

For example, USART1 is connected to APB2 bus. In order to enable the USART1 clock, the RCC_APB2ENR register needs to be configured as follows:

```
__HAL_RCC_USART1_CLK_ENABLE();
```

with STM32Cube HAL driver RCC API.

In order to disable USART1 clock during Sleep mode (to reduce power consumption) the RCC_APB2SMENR register needs to be configured as follows:

```
__HAL_RCC_USART1_CLK_SLEEP_ENABLE();
```

with STM32Cube HAL driver RCC API.

4.5.3 Peripheral clock configuration

Some peripherals have a dedicated clock source independent from the system clock, that is used to generate the clock required for their operation:

- *USB:*

  In STM32L1 series: the USB 48 MHz clock is derived from the PLL VCO clock which should be at 96 MHz.

  In STM32L4 series: the USB 48 MHz clock is derived from one of the three following sources: main PLL VCO (PLLUSB1CLK), PLLSAI1 VCO (PLLUSB2CLK), MSI clock (when the MSI clock is auto-trimmed with the LSE, it can be used by the USB OTG FS device).

- *SDIO/SDMMC:*

  In STM32L1 series: the SDIO clock (SDIOCLK) is derived from the PLL VCO clock and is equal to PLLVCO/2.

  In STM32L4 series: the SDMMC clock is derived from one of the three following sources: main PLL VCO (PLLUSB1CLK), PLLSAI1 VCO (PLLUSB2CLK), MSI clock.

- RTC and LCD:

  The RTC and the LCD Glass clock share the same clock source (RTCCLK).

  In STM32L1 series: the RTC and LCD Glass clock is derived from one of the three following sources: LSE, LSI, HSE divided by prescaler (/2, 4, 8, 16).

  In STM32L4 series: The RTC and LCD Glass clock is derived from one of the three following sources: LSE, LSI, HSE divided by 32.

- *ADC:*

  In STM32L1 series, the ADC features two clock schemes:

  – Clock for the analog circuitry: ADCCLK. This clock is always the HSI oscillator clock. A divider by 1, 2 or 4 allows to adapt the clock frequency to the device operating conditions. This configuration is done using ADC_CCR[ADCPRE] bits. The ADC clock depends also on the voltage range V_{CORE}. When product voltage range 3 is selected (V_{CORE} = 1.2 V), the ADC is low speed (ADCCLK = 4 MHz, 250 Ksps).

– Clock for the digital interface (used for register read/write access). This clock is the APB2 clock. The digital interface clock can be enabled/disabled through the RCC_APB2ENR register (ADC1EN bit) and there is a bit to reset the ADC through RCC_APB2RSTR[ADCRST] bit.

In STM32L4 series, the input clock of the two ADCs (master and slave) can be selected between two different clock sources:

– The ADCs clock can be derived (selected by software) from one of the three following sources: system clock (SYSCLK), PLLSAI1 VCO (PLLADC1CLK), PLLSAI2 VCO (PLLADC2CLK). In this mode, a programmable divider factor can be selected (1, 2, …, 256 according to bits PREC[3:0]).

– The ADC clock can be derived from the AHB clock of the ADC bus interface, divided by a programmable factor (1, 2 or 4). In this mode, a programmable divider factor can be selected (/1, 2 or 4 according to bits CKMODE[1:0]).

Refer to the STM32L1 and STM32L4 series reference manuals for more details.

- DAC:

  In STM32L4 series, in addition to the PCLK1 clock, LSI clock is used for the sample and hold operation.

- U(S)ARTs:

  In STM32L1 series, the U(S)ART clock is APB1 or APB2 clock (depending on which APB bus the U(S)ART) is mapped to.

  In STM32L4 series, the U(S)ART clock is derived from one of the four following sources: system clock (SYSCLK), HSI16, LSE, APB1 or APB2 clock (depending on which APB bus the U(S)ART is mapped to).

  Using a source clock independent from the system clock (ex: HSI16) allows to change the system clock on the fly without need to reconfigure U(S)ART peripheral baud rate prescalers.

- I2Cs:

  In STM32L1 series, the I2C clock is APB1 clock (PCLK1).

  In STM32L4 series, the I2C clock is derived from one of the three following sources: system clock (SYSCLK), HSI16, APB1 (PCLK1).

  Using a source clock independent from the system clock (ex: HSI16) allows to change the system clock on the fly without need to reconfigure I2C peripheral timing register.

4.6 PWR

In STM32L4 series the PWR controller presents some differences versus STM32L1 series, these differences are summarized in *Table 13*.

Table 13. PWR differences between STM32L1 series and STM32L4 series

PWR	STM32L1 series	STM32L4 series
Power supplies	V_{DD} = 1.8 V (at power on) or 1.65 V (at power down) to 3.6 V when the BOR is available. V_{DD} = 1.65 V to 3.6 V, when BOR is not available. V_{DD} is the external power supply for I/Os and internal regulator. It is provided externally through V_{DD} pins.	V_{DD} = 1.71 to 3.6 V: external power supply for I/Os, and internal regulator. It is provided externally through V_{DD} pins.
	V_{CORE} = 1.2 to 1.8 V V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. It is generated by a internal voltage regulator. Three V_{CORE} ranges can be selected by software depending on V_{DD} and target frequency.	V_{CORE} = 1.0 to 1.2 V V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. It is generated by a internal voltage regulator. Two V_{CORE} ranges can be selected by software depending on target frequency.
	NA	V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
	V_{DD} and V_{DDA} must be at the same voltage value.	Independent power supplies (V_{DDA}, V_{DDUSB}, V_{DDIO2}) allow to improve power consumption by running MCU at lower supply voltage than analog and USB.
	V_{SSA}, V_{DDA} = 1.8 V (at power on) or 1.65 V (at power down) to 3.6 V, when BOR is available and V_{SSA}, V_{DDA} = 1.65 to 3.6 V, when BOR is not available. V_{DDA} is the external analog power supply for ADC, DAC, reset blocks, RC oscillators and PLL. The minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.	V_{SSA}, V_{DDA} = 1.62 V (ADCs/COMPs) to 3.6 V 1.8 V (DACs/OPAMPs) to 3.6 V 2.4 V (VREFBUF) to 3.6 V V_{DDA} is the external analog power supply for A/D and D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage.
	V_{LCD} = 2.5 to 3.6 V The LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter.	V_{LCD} = 2.5 to 3.6 V (idem STM32L1 series)
	NA	V_{DDUSB} = 3.0 to 3.6 V V_{DDUSB} is the external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
	NA	V_{DDIO2} = 1.08 V to 3.6 V V_{DDIO2} is the external power supply for 14 I/Os (PG[15:2]). The V_{DDIO2} voltage level is independent from the V_{DD} voltage.

Table 13. PWR differences between STM32L1 series and STM32L4 series (continued)

PWR	STM32L1 series	STM32L4 series
Battery backup domain	NA	– RTC with backup registers (128 bytes) – LSE – PC13 to PC15 I/Os – 3 tamper pins
Power supply supervisor	Integrated POR / PDR circuitry Programmable voltage detector (PVD)	
	Brownout reset (BOR) BOR can be disabled after power-on	Brownout reset (BOR) BOR is always enabled, except in Shutdown mode
	NA	4 peripheral voltage monitoring (PVM) – PVM1 for V_{DDUSB} – PVM2 for V_{DDIO2} – PVM3/PVM4 for V_{DDA} (~1.65 V/ ~2.2 V)
Low-power modes	Sleep mode	Sleep mode
	Low-power run mode (up to 128 kHz) Low-power sleep mode (up to 128 kHz)	Low-power run mode (up to 2 MHz) Low-power sleep mode (up to 2 MHz) System clock is limited to 2 MHz, but I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz.
	Stop mode	Stop 0, Stop 1 and Stop 2 mode Some additional functional peripherals (cf wakeup source)
	Standby mode (V_{CORE} domain powered off)	Standby mode (V_{CORE} domain powered off) with new features: – BOR is always ON – SRAM2 content can be preserved – Pull-up or pull-down can be applied on each I/O
	NA	Shutdown mode (V_{CORE} domain powered off and power monitoring off)

Table 13. PWR differences between STM32L1 series and STM32L4 series (continued)

PWR	STM32L1 series	STM32L4 series
Wake-up sources	Sleep mode Any peripheral interrupt/wakeup event	Sleep mode Any peripheral interrupt/wakeup event
	Stop mode Any EXTI line event/interrupt BOR, PVD, COMP, RTC, USB, IWDG	Stop mode Any EXTI line event/interrupt BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, SWP, LPTIM, LCD
	Standby mode 3 WKUP pins rising edge RTC event External reset in NRST pin IWDG reset	Standby mode 5 WKUP pins rising or falling edge RTC event External reset in NRST pin IWDG reset
	NA	Shutdown mode 5 WKUP pins rising or falling edge RTC event External reset in NRST pin
Wake-up clocks	Wakeup from Stop mode MSI (all ranges up to 4.1 MHz)	Wakeup from Stop mode HSI16 16 MHz or MSI (all ranges up to 48 MHz) allowing 5 µs wakeup at high speed without waiting for PLL startup time.
	Wakeup from Standby mode MSI 2.097 MHz	Wakeup from Standby mode MSI (ranges from 1 to 8 MHz)
	NA	Wakeup from Shutdown mode MSI 4 MHz
Configuration	-	In STM32L4 series the registers are different: From 2 registers in STM32L1 series to 23 registers in STM32L4 series – 4 control registers – 2 status registers – 1 status clear register – 2 registers per GPIO port (A,B,..H) for controlling pull-up and pull-down (16registers) Most configuration bits from STM32L1 series can be found in STM32L4 series (but sometime may have different programming mode)

Color key:

= New feature or new architecture (difference between STM32L1 and STM32L4 series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32L1 and STM32L4 series highlight

4.7 RTC

The STM32L4 and STM32L1 series implement almost the same feature on the RTC.

Table 14. RTC differences between STM32L1 series and STM32L4 series

RTC	STM32L1 series	STM32L4 series
Features	Coarse digital calibration (kept for compatibility only. New developments should only use smooth calibration).	Only smooth calibration available.
Configuration	-	– RTC_CR/DCE not available – RTC_CALIB register not available – RTC_TAFCR (L1) -> RTC_TAMPCR (L4) Except bit ALARMOUTTYPE available on RTC_OR/RTC_ALARM_TYPE
Color key: = Same feature, but specification change or enhancement = Feature not available (NA)		

For more information about STM32L4 series RTC features, please refer to RTC section of STM32L4 series reference manuals.

4.8 SYSCFG and RI

The STM32L4 and STM32L1 series implement almost the same feature on the SYSCFG.

The table below shows the differences.

Table 15. SYSCFG differences between STM32L1 series and STM32L4 series

SYSCFG/RI	STM32L1 series	STM32L4 series
RI features	TIM2/TIM3/TIM4's input captures 1,2,3 and four routing selections from selectable I/Os – Routing of internal reference voltage VREFINT to selectable I/Os for all packages – Up to 40 external I/Os + 3 internal nodes (internal reference voltage + temperature sensor + V_{DD} and $V_{DD}/2$ measurement by VCOMP) can be used for data acquisition purposes in conjunction with the ADC interface – Input and output routing of COMP1 and COMP2	The RI IO switches control used for the Touch Sense application has been replaced by a dedicated peripheral (TSC) in STM32L4 series. The remaining switches control (for ADC, COMP) and internal interconnects are managed inside each specific peripheral in STM32L4 series. The overall functionality is not equivalent.
Configuration	-	Most registers from STM32L1 series can be found in STM32L4 series: – SYSCFG_MEMRMP: bits[9:8] (BOOT_MODE) have no equivalent in STM32L4 series – SYSCFG_PMC: no equivalent in STM32L4 series – SYSCFG_EXTICR1/2/3/4: values for each EXTIx[3:0] mapping to PAx,..PHx is different in STM32L4 series.
Color key: = Same feature, but specification change or enhancement = Feature not available (NA)		

4.9 GPIO

The STM32L4 series GPIO peripheral embeds identical features compared to STM32L1 series.

Minor adaptation of the code written for the STM32L1 series using the GPIO may be required in STM32L4 series due to:

- Mapping of particular function on different GPIOs (see pinout difference in *Section 2: Hardware migration*)
- Alternate function selection differences (AFSELy[3:0] in registers GPIOx_AFRL and GPIOx_AFRH)

Below are the main GPIO features:

- GPIO mapped on AHB bus for better performance
- I/O pin multiplexer and mapping: pins are connected to on-chip peripherals/modules through a multiplexer that allows only one peripheral alternate function (AF) connected to an I/O pin at a time. In this way, there cannot be any conflict between peripherals sharing the same I/O pin.
- More possibilities and features for I/O configuration

For more information about STM32L4 series GPIO programming and usage, please refer to the "I/O pin multiplexer and mapping" subsection in the GPIO section of the STM32L4 reference manuals and to the product datasheets for detailed description of the pinout and alternate function mapping.

4.10 EXTI source selection

The external interrupt/event controller (EXTI) is very similar on both STM32L1 and STM32L4 series. The table below shows the main differences.

Table 16. EXTI differences between STM32L1 series and STM32L4 series

EXTI	STM32L1 series	STM32L4 series
Nb of event/interrupt lines	Up to 24 lines	Up to 40 lines (14 direct, 26 configurable)
Configuration	-	The selection of EXTI line source is performed through EXTIx bits in SYSCFG_EXTICRx registers (in STM32L1 and STM32L4 series). However, the mapping of the EXTICRx registers has been changed.
Color key: = Same feature, but specification change or enhancement		

4.11 FLASH

The table below presents the difference between the FLASH interface of STM32L1 series and STM32L4 series.

The STM32L4 instantiates a different FLASH module both in terms of architecture/technology and interface, consequently the STM32L4 series Flash memory programming procedures and registers are different from the STM32L1 series, and any code written for the Flash memory interface in the STM32L1 series needs to be rewritten to run in STM32L4 series.

For more information on programming, erasing and protection of the STM32L4 series Flash memory, please refer to the STM32L4 reference manuals.

Table 17. FLASH differences between STM32L1 series and STM32L4 series

FLASH	STM32L1 series	STM32L4 series
Main/Program memory	0x0800 0000 – (up to) 0x0805 FFFF	0x0800 0000 - up to 0x080F FFFF
	Up to 512 Kbyte Split in 2 Banks Each bank: up to 256 Kbyte Sector size = 4 Kbyte: 16 Pages of 256 bytes Programming granularity: 32-bit Read granularity: 64/32-bit	Up to 1 Mbyte Split in 2 Banks Each bank: 256 pages of 2 Kbyte Each page: 8 rows of 256 Bytes Programming and Read granularity 72-bit (incl 8 ECC bits)
Features	Read while write (RWW) Dual bank boot ECC (data EEPROM only)	Read while write (RWW) Dual bank boot ECC
Wait State	Up to 1 (depending on the supply voltage and frequency)	Up to 4 (depending on the core voltage and frequency)
ART Accelerator™	NA	Allowing 0 wait state when executing from the cache.
Data EEPROM memory	0x0808 0000 – 0x0808 0FFF (Cat.1,2) 0x0808 0000 – 0x0808 1FFF (Cat.3) 0x0808 0000 – 0x0808 2FFF (Cat.4) 0x0808 0000 – 0x0808 3FFF (Cat.5)	N/A can be emulated by SW
System memory	0x1FF0 0000 - 0x1FF0 0FFF (Cat1,2) 0x1FF0 0000 - 0x1FF0 1FFF (Cat.3,4,5)	0x1FFF 0000 – 0x1FFF 6FFF (bank1) 0x1FFF 8000 – 0x1FFF EFFF (bank2)
One Time programmable (OTP)	NA	0x1FFF 7000 - 0x1FFF 73FF (bank1)
Option Bytes	0x1FF8 0000 - 0x1FF8001F (all Cat.x) 0x1FF8 0080 - 0x1FF8 009F (Cat.4,5)	0x1FFF 7800 - 0x1FFF 780F (bank1) 0x1FFF F800 - 0x1FFF F80F (bank2)
Flash memory interface	0x4002 3C00 - 0x4002 3FFF	0x4002 2000 - 0x4002 23FF
	-	Different from STM32L1 series

Table 17. FLASH differences between STM32L1 series and STM32L4 series (continued)

FLASH	STM32L1 series	STM32L4 series
Erase granularity	Program memory: Mass/Page (256 bytes) DATA EEPROM memory: byte/ halfword/ word / double word	Page erase (2Kbytes), Bank erase and Mass erase (both banks)
Read protection (RDP)	Level 0 no protection RDP = 0xAA	
	Level 1 memory protection RDP ≠ (Level 2 & Level 0)	
	Level 2 RDP = 0xCC (1)	
Proprietary code readout protection (PCROP)	Granularity: 1 sector (4 Kbyte)	2 PCROP areas (1 per bank) Granularity: 64-bit PCROP_RDP option: PCROP area preserved when RDP level decreased.
Write protection (WRP)	Granularity: 1 sector (4 Kbyte)	4 write protection areas (2 per bank) Granularity: 2 Kbyte
User Option bytes	nRST_STOP	nRST_STOP
	nRST_STDBY	nRST_STDBY
	IWDG_SW	IWDG_SW
	NA	IWDG_STOP, IWDG_STDBY
	NA	WWDG_SW
	BOR_LEV[3:0]	BOR_LEV[2:0]
	nBFB2	BFB2
	NA	nBOOT1
	NA	SRAM2_RST, SRAM2_PE
	NA	DUAL BANK

Color key:

= New feature or new architecture (difference between STM32L1 and STM32L4 series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32L1 and STM32L4 series highlight

4.12 U(S)ART

The STM32L4 series implement several new features on the U(S)ART compared to STM32L1 series.

The table below shows the differences.

Table 18. U(S)ART differences between STM32L1 series and STM32L4 series

U(S)ART	STM32L1 series	STM32L4 series
Instances	3 x USART 2 x UART	3 x USART 2 x UART 1 x LPUART
Baud rate	Up to 4 Mbit/s (when the clock frequency is 32 MHz and oversampling is by 8)	Up to 10 Mbit/s (when the clock frequency is 80 MHz and oversampling is by 8)
Clock	Single clock domain	Dual clock domain allowing: – UART functionality and wakeup from Stop mode – Convenient baud rate programming independent from the PCLK reprogramming
Data	**Word length**: Programmable (8 or 9 bits)	**Word length**: Programmable (7, 8 or 9 bits) Programmable data order with MSB-first or LSB-first shifting
Interrupt	10 interrupt sources with flags	14 interrupt sources with flags
Features	RS232 hardware flow control (CTS/RTS) Continuous communication using DMA Multiprocessor communication Single-wire half-duplex communication IrDA SIR ENDEC block LIN mode SPI master	
	Smartcard mode T = 0 and T = 1 is to be implemented by software. Number of stop bits: 0.5, 1, 1.5, 2	Smartcard mode T = 0, T=1 are supported. (features are added to support T = 1 such as receiver timeout, block length, end of block detection, binary data inversion etc...). Number of stop bits: 1, 1.5, 2

Table 18. U(S)ART differences between STM32L1 series and STM32L4 series (continued)

U(S)ART	STM32L1 series	STM32L4 series
Features	NA	Wakeup from STOP mode (Start Bit, Received Byte, Address match). Support for ModBus communication: – Timeout feature – CR/LF character recognition. Receiver timeout interrupt (except LPUART). Auto baud rate detection (except LPUART). Driver enable. Swappable Tx/Rx pin configuration. LPUART does not support Synchronous mode (SPI master), Smartcard mode, IrDA, LIN, ModBus, Receiver timeout interrupt, Auto baud rate detection.
Configuration	-	L1 registers and associated bits are not identical in STM32L4 series. Please refer to STM32L4 reference manuals for details.

Color key:

= New feature or new architecture (difference between STM32L1 and STM32L4 series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32L1 and STM32L4 series highlight

4.13 I2C

The STM32L4 implements a different I2C peripheral allowing easy software management.

The table below shows the differences.

Table 19. I2C differences between STM32L1 series and STM32L4 series

I2C	STM32L1 series	STM32L4 series
Instances	x2 (I2C1, I2C2)	x3 (I2C1, I2C2, I2C3)
Features	7-bit and 10-bit addressing mode SMBus Standard mode (Sm, up to 100 kHz) Fast mode (Fm, up to 400 kHz)	
	NA	Fast mode Plus (Fm+, up to 1 MHz) Independent clock Wakeup from Stop on address match

Table 19. I2C differences between STM32L1 series and STM32L4 series (continued)

I2C	STM32L1 series	STM32L4 series
Configuration	-	Register configuration is very different in STM32L1 and STM32L4 series. Please refer to STM32L4 series reference manuals for details.
Color key: = New feature or new architecture (difference between STM32L1 and STM32L4 series) = Same feature, but specification change or enhancement = Difference between STM32L1 and STM32L4 series highlight		

4.14 SPI

The STM32L4 and STM32L1 series implement almost the same features on the SPI (apart from I2S).

The table below shows the differences.

Table 20. SPI differences between STM32L1 series and STM32L4 series

SPI	STM32L1 series	STM32L4 series
Instances	x3 (SPI1, SPI2, SPI3)	x3 (SPI1, SPI2, SPI3)
Features	SPI + I2S	I2S feature is not supported by SPI in STM32L4 series, 2 SAI interfaces are available instead.
Data size	Fixed, configurable to 8 or 16 bits	Programmable from 4 to 16-bit
Data buffer	Tx & Rx 16-bit buffers (single data frame)	32-bit Tx & Rx FIFOs (up to 4 data frames)
Data packing	No (16-bit access only)	Yes (8-bit, 16-bit or 32-bit data access, programmable FIFOs data thresholds).
Mode	SPI TI mode SPI Motorola mode	SPI TI SPI Motorola mode NSSP mode
Speed	16 MHz (core at 32 MHz)	TBD
Configuration	-	The data size and Tx/Rx flow handling are different in STM32L1 and STM32L4 series hence requiring different SW sequences.
Color key: = New feature or new architecture (difference between STM32L1 and STM32L4 series) = Same feature, but specification change or enhancement = Difference between STM32L1 and STM32L4 series highlight		

Migrating from I2S to SAI:

STM32L4 does not include I2S interface part of the SPI peripheral, instead it includes two serial audio interfaces.

The table below shows main differences between I2S and SAI.

Table 21. Migrating from I2S to SAI

I2S/SAI	STM32L1 series (I2S)	STM32L4 series (SAI)
Instances	x2	x2 (SAI1, SAI2)
Features	Full-duplex communication.	Two independent audio sub-blocks (per SAI) which can be transmitters or receivers with their respective FIFOs.
	Master or slave operations.	Synchronous or asynchronous mode between the audio sub-blocks. Possible synchronization between multiple SAIs. Master or slave configuration independent for both audio sub-blocks.
	8-bit programmable linear prescaler to reach accurate audio sample frequencies (from 8 kHz to 192 kHz).	Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
	Data format may be 16-bit, 24-bit or 32-bit. Data direction is always MSB first.	Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit. First active bit position in the slot is configurable. LSB first or MSB first for data transfer.
	Channel length is fixed to 16-bit (16-bit data size) or 32-bit (16-bit, 24-bit, 32-bit data size) by audio channel.	Up to 16 slots available with configurable size. Number of bits by frame can be configurable. Frame synchronization active level configurable (offset, bit length, level). Stereo/mono audio frame capability.
	Programmable clock polarity (steady state)	Communication clock strobing edge configurable (SCK).
	16-bit register for transmission and reception with one data register for both channel sides.	8-word integrated FIFOs for each audio sub-block (facilitating interrupt mode).
	Supported I2S protocols: – I2S Philips standard – MSB-justified standard (left-justified) – LSB-justified standard (right-justified) – PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame).	Audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM (up to 16 channels), AC'97. SPDIF output.
	DMA capability for transmission and reception (16-bit wide)	2-channel DMA per SAI

Table 21. Migrating from I2S to SAI (continued)

I2S/SAI	STM32L1 series (I2S)	STM32L4 series (SAI)
Features	Master clock may be output to drive an external audio component. Ratio is fixed at 256 × Fs (where Fs is the audio sampling frequency)	
	Interruption sources when enabled: – Errors – Tx buffer empty, Rx buffer not empty.	Interruption sources when enabled: – Errors – FIFO requests.
	Error flags with associated interrupts if enabled respectively: – Overrun and underrun detection, – Anticipated frame synchronization signal detection in slave mode, – Late frame synchronization signal detection in slave mode,	Idem STM32L1 series + Protection against misalignment in case of underrun and overrun.
Configuration	-	There is no compatibility between STM32L1 series I2S and STM32L4 series SAI. User will have to configure the SAI interface for the target protocol. Please refer to reference manuals for details.
Color key: = New feature or new architecture (difference between STM32L1 and STM32L4 series) = Same feature, but specification change or enhancement = Difference between STM32L1 and STM32L4 series highlight		

The SAI peripheral improves robustness of communication in slave mode compared to I2S peripheral (in case of data clock glitch for example)

In master mode, while migrating an application from STM32L1 to STM32L4 series, the user should review the possible master clock (MCLK), data bit clock (SCK) and frame synchronization (FS) frequency reachable using STM32L4 PLL multiplication factors and SAI internal clock divider for a given external oscillator which can be different than with STM32L1 series I2S.

In STM32L4 MCUs, the SAI1 and SAI2 input clocks are derived (selected by software) from one of the four following sources:

- an external clock mapped on SAI1_EXTCLK for SAI1 and SAI2_EXTCLK for SAI2.
- PLLSAI1 (P) divider output (PLLSAI1CLK)
- PLLSAI2 (P) divider output (PLLSAI2CLK)
- main PLL (P) divider output (PLLSAI3CLK)

When the clock is derived from one of the three internal PLLs, the three PLL inputs are either HSI16, HSE or MSI (between 4 and 8 MHz) divided by a programmable factor PLLM (from 1 to 8). This input is then multiplied by PLLN (from 8 to 86) to reach PLL VCO frequency (should be between 64 and 344 MHz). It is finally divided by PLLP (7 or 17) to provide the input clock for SAI (max. 80 MHz)

When the Master clock MCLK is used by the external slave audio peripheral, the PLL output is divided by SAI internal master clock divider factor (1, 2, 4, 6, 8, 10, ..., 30) to provide the master clock (MCLK). The data bit clock is then derived from MCLK following the formula:

$$SCK = MCLK \times (FRL + 1) / 256$$

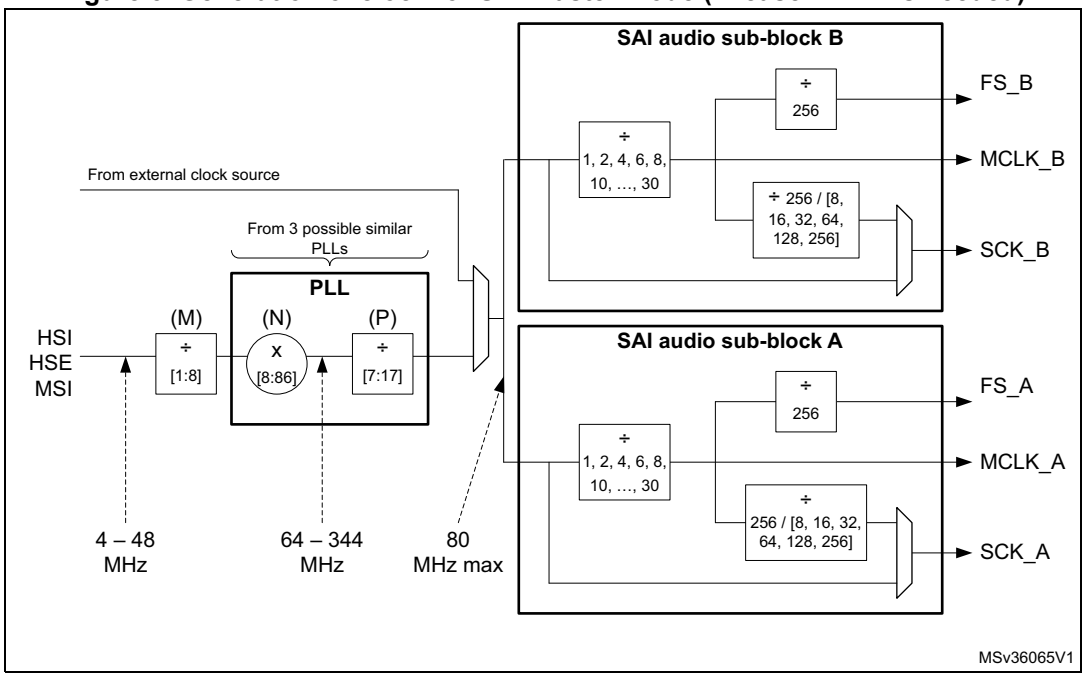
where (FRL + 1) = 8, 16, 32, 64, 128, 256:

- FRL is the number of bit clock cycles -1 in the audio frame.
- (FRL + 1) should be a power of 2 higher or equal to 8.

SCK can also be directly connected to input clock of SAI when MCLK output is not needed.

The frame synchronization (FS) frequency is always MCLK / 256.

Figure 5. Generation of clock for SAI master mode (in case MCLK is needed)



Please refer to reference manuals for more details.

4.15 CRC

The cyclic redundancy check (CRC) calculation unit is very similar in STM32L1 and STM32L4 series.

The table below shows the differences.

Table 22. CRC differences between STM32L1 series and STM32L4 series

CRC	STM32L1 series	STM32L4 series
Features	Single input/output 32-bit data register. CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size. General-purpose 8-bit register (can be used for temporary storage).	
	Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7. Handles 32-bit data size.	Fully programmable polynomial with programmable size (7, 8, 16, 32bits) Handles 8-,16-, 32-bit data size. Programmable CRC initial value. Input buffer to avoid bus stall during calculation. Reversibility option on I/O data.
Configuration	-	Configuration registers in STM32L1 series are identical in STM32L4 series. STM32L4 series includes additional registers for new features. Please refer to reference manuals for details.
Color key: = New feature or new architecture (difference between STM32L1 and STM32L4 series)		

4.16 AES

The STM32L4 series implement several new features on the AES compared to STM32L1 series.

The table below shows the differences.

Table 23. AES differences between STM32L1 series and STM32L4 series

AES	STM32L1 series	STM32L4 series
Features	128-bit register for storing the encryption or derivation key (4x 32-bit registers).	256-bit register for storing the encryption, decryption or derivation key (8x 32-bit registers).
Mode	Electronic codebook (ECB). Cipher block chaining (CBC). Counter mode (CTR).	Electronic codebook (ECB). Cipher block chaining (CBC). counter mode (CTR). Galois counter mode (GCM). Galois message authentication code mode (GMAC). Cipher message authentication code mode (CMAC).
Key length	128-bit	128-bit, 256-bit
Configuration	-	All registers and programming bits in STM32L1 series can be found in STM32L4 series.

Color key:

= New feature or new architecture (difference between STM32L1 and STM32L4 series)

= Same feature, but specification change or enhancement

4.17 LCD

The STM32L4 series LCD implements the same features than the STM32L1 series except for additional internal output buffers that allow to further improve contrast (it is possible to use output buffers instead of high drive resistive network).

All programmable registers and associated bits in STM32L1 series are equivalent in STM32L4 series. However, due to the fact that VLCD pin is implemented as alternate function in STM32L4 series (contrary to STM32L1 series), a specific SW sequence is required to configure the LCD when the step-up converter is used as power source.

Please refer to reference manuals for more details.

4.18 USB

The STM32L4 and STM32L1 series implement different USB peripherals.

While STM32L1 series implements a USB FS device interface, the STM32L4 series implements a USB OTG FS interface.

Most features supported by STM32L1 series are also supported by STM32L4 series.

The key differences are listed below.

Table 24. USB differences between STM32L1 series and STM32L4 series

USB	STM32L1 series	STM32L4 series
Features	Universal serial bus Revision 2.0.	Universal serial bus Revision 2.0, including link power management (LPM) support
	NA	Full support for the USB on-the-go (USB OTG).
	FS mode: – 1 bidirectional control endpoint – 7 IN endpoints (Bulk, Interrupt, Isochronous) – 7 OUT endpoints (Bulk, Interrupt, Isochronous).	FS mode: – 1 bidirectional control endpoint – 5 IN endpoints (Bulk, Interrupt, Isochronous) – 5 OUT endpoints (Bulk, Interrupt, Isochronous).
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D+ (USB_DP) line.	
	NA	Attach Detection Protocol (ADP) Battery Charging Detection (BCD)
	NA	Independent V_{DDUSB} power supply allowing lower V_{DDCORE} while using USB.
Mapping	APB1	AHB2
Buffer memory	512bytes (endpoint buffers and buffer descriptors structure).	1.25Kbytes data FIFOs Management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO.
Low-power modes	USB suspend and resume	USB suspend and resume. Link power management (LPM) support.
Configuration	-	In STM32L4 series the registers are different. Please refer to reference manuals for details.

Color key:

= New feature or new architecture (difference between STM32L1 and STM32L4 series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32L1 and STM32L4 series highlight

4.19 ADC

The table below presents the differences between the ADC peripheral of STM32L1 series and STM32L4 series, these differences are the following:

- New digital interface
- New architecture and new features.

Table 25. ADC differences between STM32L1 series and STM32L4 series

ADC	STM32L1 series		STM32L4 series	
ADC Type	SAR structure			
Instances	ADC1		ADC1 / ADC2 / ADC3	
Maximum sampling frequency	1 Msps		5.1 Msps (fast channels) 4.8 Msps (slow channels)	
Number of channels	up to 42 channels		Up to 19 channels per ADC	
Resolution	12-bit		12-bit + digital oversampling up to 16-bit	
Conversion Modes	Single / continuous / scan / discontinuous		Single / continuous / scan / discontinuous dual mode	
DMA	Yes			
External Trigger	Yes			
	External event for regular group TIM9_CC2 TIM9_TRGO TIM2_CC3 TIM2_CC2 TIM3_TRGO TIM4_CC4 TIM2_TRGO TIM3_CC1 TIM3_CC3 TIM4_TRGO TIM6_TRGO EXTI line11	External event for injected group TIM9_CC1 TIM9_TRGO TIM2_TRGO TIM2_CC1 TIM3_CC4 TIM4_TRGO TIM4_CC1 TIM4_CC2 TIM4_CC3 TIM10_CC1 TIM7_TRGO EXTI line15	External event for regular group: TIM1 CC1 TIM1 CC2 TIM1 CC3 TIM2 CC2 TIM3 TRGO TIM4 CC4 EXTI line 11 TIM8_TRGO TIM8_TRGO2 TIM1_TRGO TIM1_TRGO2 TIM2_TRGO TIM4_TRGO TIM6_TRGO TIM15_TRGO TIM3_CC4	External event for injected group: TIM1 TRGO TIM1 CC4 TIM2 TRGO TIM2 CC1 TIM3 CC4 TIM4 TRGO EXTI line15 TIM8_CC4 TIM1_TRGO2 TIM8_TRGO TIM8_TRGO2 TIM3_CC3 TIM3_TRGO TIM3_CC1 TIM6_TRGO TIM15_TRGO
Supply requirement	1.8 V to 3.6 V		1.62 V to 3.6 V Independent power supply (V_{DDA})	
Reference Voltage	External		Reference voltage for STM32L4 series external (2.0 V to V_{DDA}) or internal (2.048 V or 2.5 V)	

Table 25. ADC differences between STM32L1 series and STM32L4 series (continued)

ADC	STM32L1 series	STM32L4 series
Electrical Parameters	1.45 mA (max.), 1.0 mA (Typ.)	Consumption proportional to conversion speed: 200 µA/Msps (Typ.)
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	
Color key: = New feature or new architecture (difference between STM32L1 and STM32L4 series) = Same feature, but specification change or enhancement		

4.20 DAC

The STM32L4 series implement some enhanced DAC compared to STM32L1 series.

The table below shows the differences.

Table 26. DAC differences between STM32L1 series and STM32L4 series

DAC	STM32L1 series	STM32L4 series
Instances	x2	
Resolution	12-bit	
Features	Left or right data alignment in 12-bit mode Noise-wave and triangular-wave generation Dual DAC channel for independent or simultaneous conversions	
	NA	Buffer offset calibration. DAC_OUTx can be disconnected from output pin. Sample and hold mode for low power operation in Stop mode.
DMA	Yes	
External Trigger	Yes	
	TIM6 TRGO TIM7 TRGO TIM9 TRGO TIM2 TRGO TIM4 TRGO EXTI line9 SW TRIG	TIM6 TRGO TIM8 TRGO TIM7 TRGO TIM5 TRGO TIM2 TRGO TIM4 TRGO EXTI line9 SW TRIG
Supply requirement	1.8 V to 3.6 V	1.8 V to 3.6 V Independent power supply (V_{DDA})
Reference Voltage	External	Reference voltage for STM32L4 series external (1.8 V to V_{DDA}) or internal (2.048 V or 2.5 V)

Table 26. DAC differences between STM32L1 series and STM32L4 series (continued)

DAC	STM32L1 series	STM32L4 series
Configuration	-	SW compatible except for output buffer management.

Color key:

= New feature or new architecture (difference between STM32L1 and STM32L4 series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32L1 and STM32L4 series highlight

4.21 COMP

The table below presents the differences between the COMP interface of STM32L1 series and STM32L4 series:

Table 27. COMP differences between STM32L1 series and STM32L4 series

COMP	STM32L1 series	STM32L4 series
Type	COMP1 fixed threshold COMP2 rail-to-rail	COMP1, COMP2 rail-to-rail
Inputs	**COMP1:** – 25 (Cat.1,2) (24 ext IO + T sensor) – 32 (Cat.3,4,5) (29 ext IO + T sensor + OPAMP1/2) **COMP2**: Non inverting: – 2 (Cat.1,2) (PB4, PB5) – 4 (Cat3,4,5) (PB4, PB5, PB6, PB7) Inverting: – 7 (PB3, DAC_OUT1/2, V_{REFINT} x 1, 3/4, 1/2, 1/4)	**COMP1:** Non Inverting: – 2 (PC5, PB2) Inverting: – 8 (PB1,PC3, DAC_OUT1/2, V_{REFINT} x 1, 3/4, 1/2, 1/4) **COMP2**: Non Inverting: – 2 (PB4, PB6) Inverting: – 8 (PB3, PB7, DAC_OUT1/2, V_{REFINT} x 1, 3/4, 1/2, 1/4)
Outputs	Generation of input capture and OCREF clear signals for TIM2, TIM3, TIM4 and input capture for TIM10. Generation of wakeup interrupt or events (EXTI line).	Generation of break input signals for TIM1/TIM8 through GPIO alternate function. Generation of wakeup interrupt or events (EXTI line).
Features	Window comparator	
	NA	Output with blanking source Programmable hysteresis
	Programmable speed/consumption (COMP2)	Programmable speed/consumption (COMP1/COMP2)

Table 27. COMP differences between STM32L1 series and STM32L4 series (continued)

COMP	STM32L1 series	STM32L4 series
Supply requirement	1.65 V to 3.6 V	1.62 V to 3.6 V
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	
Color key: = New feature or new architecture (difference between STM32L1 and STM32L4 series) = Same feature, but specification change or enhancement = Feature not available (NA)		

4.22 OPAMP

The STM32L4 series implement some enhanced OPAMPs compared to STM32L1 series.

The table below shows the differences.

Table 28. OPAMP differences between STM32L1 series and STM32L4 series

OPAMP	STM32L1 series	STM32L4 series
Instances	x3	x2
Features	Rail-to-rail input and output voltage range Low input bias current Low input offset voltage Low power mode Fast wakeup time Gain bandwidth of 1 MHz	
	NA	Programmable gain amplifier (PGA)
Configuration	-	The configuration registers are not organized in the same way in the STM32L4 series and in the STM32L1 series.
Color key: = New feature or new architecture (difference between STM32L1 and STM32L4 series) = Same feature, but specification change or enhancement = Feature not available (NA) = Difference between STM32L1 and STM32L4 series highlight		

5 Revision history

Table 29. Document revision history

Date	Revision	Changes
16-Jul-2015	1	Initial release.
23-Nov-2015	2	*Section 4.2: Memory mapping* updated: Stop 0 mode added for content preservation *Table 13: PWR differences between STM32L1 series and STM32L4 series* updated: Stop 0 mode added